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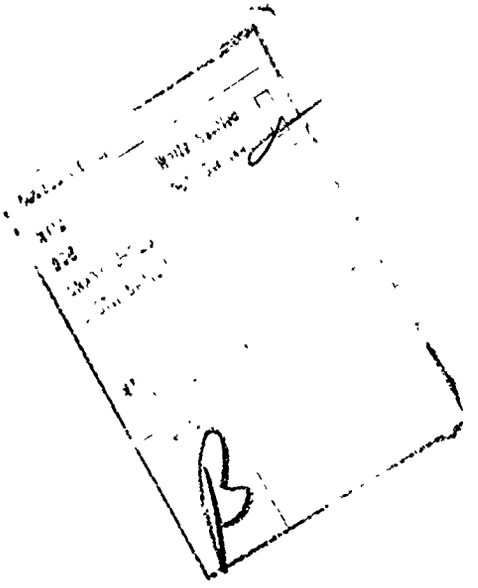
INTEGRATED CIRCUIT ELECTROMAGNETIC SUSCEPTIBILITY INVESTIGATION - PHASE II

PULSE INTERFERENCE STUDY

MCDONNELL DOUGLAS ASTRONAUTICS COMPANY - EAST

MCDONNELL DOUGLAS
CORPORATION



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INTEGRATED CIRCUIT ELECTROMAGNETIC SUSCEPTIBILITY INVESTIGATION PHASE II

12 JULY 1974

MDC-E1102

PULSE INTERFERENCE STUDY

31 p.

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DAHLGREN, VA. 22448
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PREFACE

This document is one of eight task-oriented reports prepared under Contract No. N00178-73-C-0362 for the U. S. Naval Weapons Laboratory, Dahlgren, Virginia 22448. The McDonnell Douglas Astronautics Company personnel involved were:

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1. INTRODUCTION AND SUMMARY

The Integrated Circuit Electromagnetic Susceptibility Investigation is concerned with the adverse effects that electromagnetic environments can induce in the integrated circuits used in Navy electronic equipment. Previous work [1, 2, 3] has demonstrated susceptibility of representative linear and digital integrated circuits under CW stimulus at five microwave frequencies: .22, .91, 3.0, 5.6, and 9.1 GHz. Because most of the severe electromagnetic environments to be encountered by sensitive electronic systems will be due to pulsed radar transmitters which typically radiate high peak power in short pulses (1000 times higher power than the average level), it is important to determine the response of the same representative linear and digital devices to pulsed RF signals.

A linear 741 operational amplifier and a digital 7400 NAND gate were tested with injected RF pulses as short as one microsecond and at pulse repetition frequencies up to 10 KHz. The basic rectification mechanism which converts the pulsed RF energy to an equivalent video pulse (envelope of the RF pulse) was found to have no minimum time delay (down to one microsecond), and the peak value of the detected pulse corresponds to the level predicted by the CW measurements. Response of the individual circuit to the induced video pulse does depend on the inherent speed capabilities of the device, however. The switching speed and propagation delay time of the 7400 NAND gate are the limiting factors for this device, but the one microsecond pulse width did not approach these limitations. The output slew rate and output saturation levels limit the response of the 741 operational amplifier with respect to rise time and maximum amplitude.

The implications of an interfering signal which is sometimes present and sometimes absent are addressed for the two general divisions of digital and linear circuits. For digital circuits, the problems of bit errors and propagation delays

are discussed. For linear circuits, the concepts of average response and signal-to- noise ratio degradation are covered.

2. PULSED RF INTERFERENCE MEASUREMENTS

The basic test plan for this work was to inject pulse modulated RF signals into the ports of the 741 operational amplifier and 7400 NAND gate which had previously been demonstrated [3] to be susceptible. The output response was monitored with a high speed oscilloscope and photographs of the device response serve as the data format. Detailed test set-ups are documented elsewhere [4], but figure 1 shows the special IC test fixture developed under this contract for carefully controlling the RF transmission and injection parameters.

2.1 7400 NAND Gate Results - Two different test configurations were selected for the 7400 NAND gate as illustrated in figure 2. In both of these configurations, the injected RF signal has been shown to cause adverse effects up to and including complete change of logic state [3]. The conversion mechanism has been shown [5] to be rectification in the parasitic collector isolation junctions of the device. Figure 3 shows typical output voltage response to CW stimulus for both configurations as measured with an RF signal at 220 MHz.

Injecting RF pulses at each of the four test frequencies of .22, .91, 3.0, and 5.6 GHz (the 7400 is not susceptible at 9.1 GHz) demonstrated that the peak interference effect corresponds to the peak RF power level according to the predictions from CW response such as those shown in figure 3. Figure 4 displays typical observations of induced pulses on the device output. In all cases tested, the device response due to RF pulses was identical to the video pulse response for pulse widths down to one microsecond. In view of the relatively clean rise and fall time properties of the induced pulse, it is not surprising that there are no cumulative effects due to high PRF rates as shown in figure 5 for a 10 KHz pulse repetition frequency. Table 1 summarizes the observed pulse effects in the 7400 NAND gate.

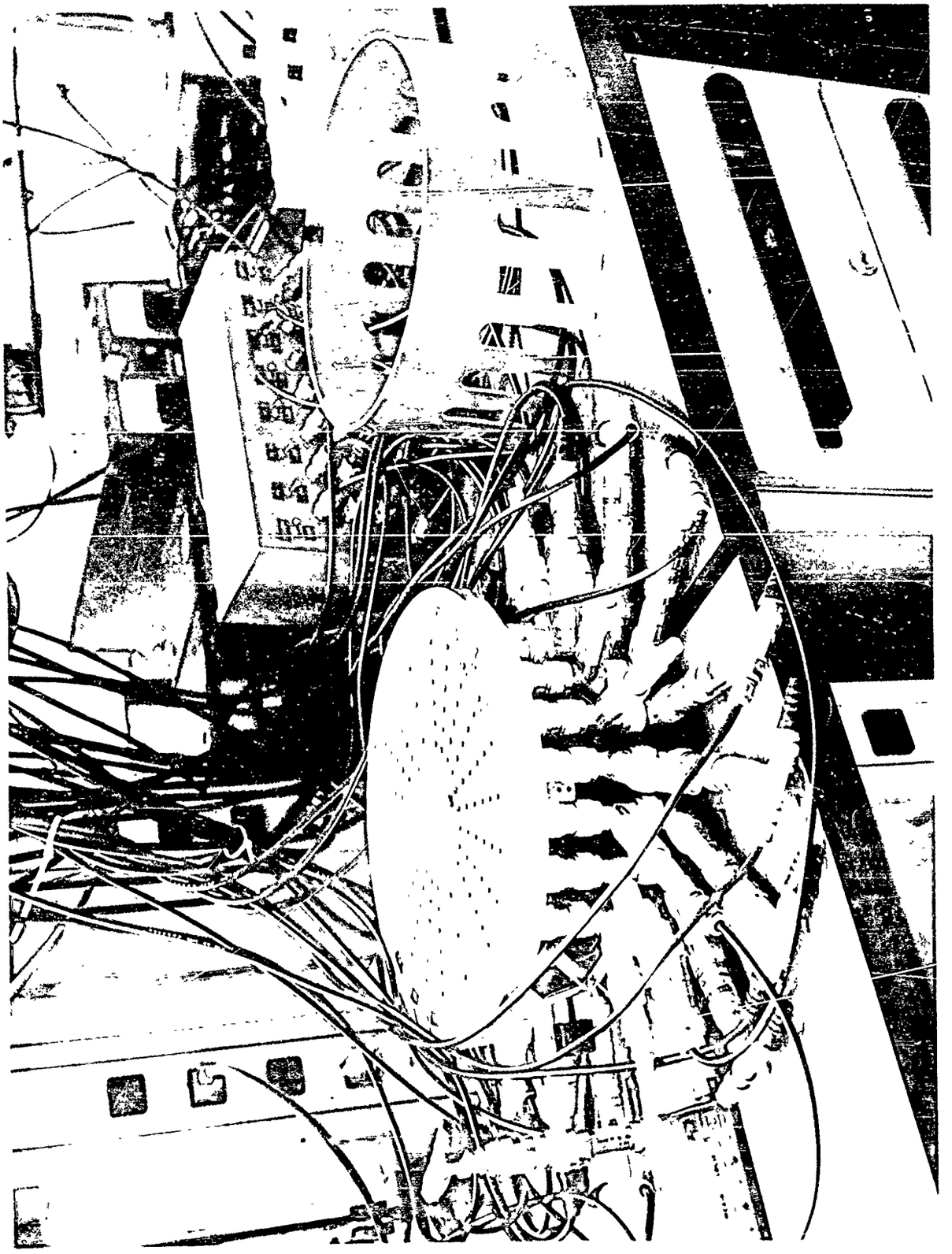
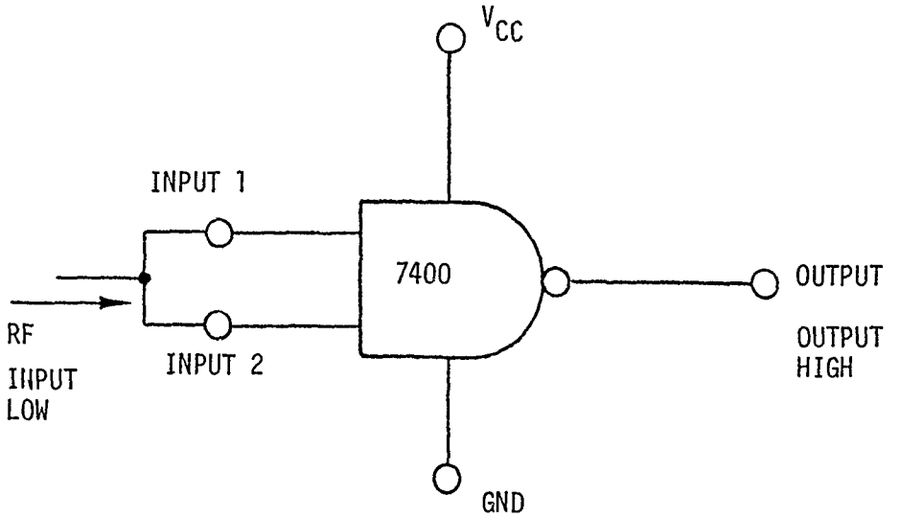
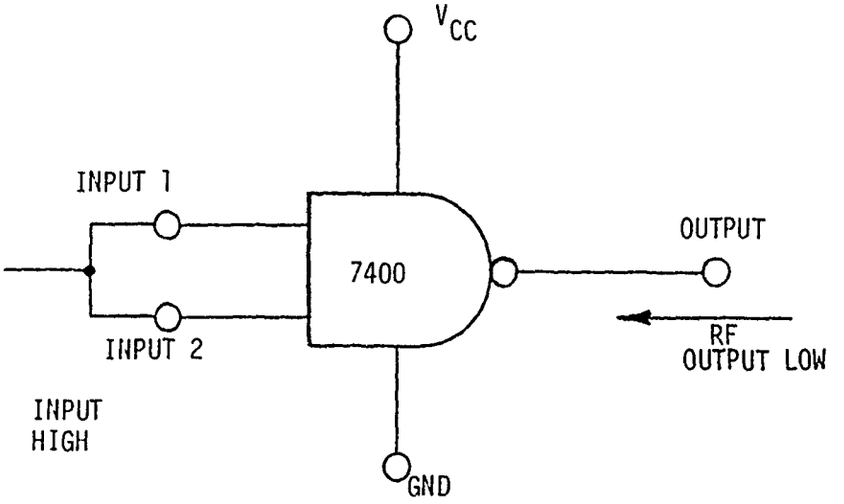


FIGURE 1 PHOTOGRAPH OF I C TEST FIXTURE

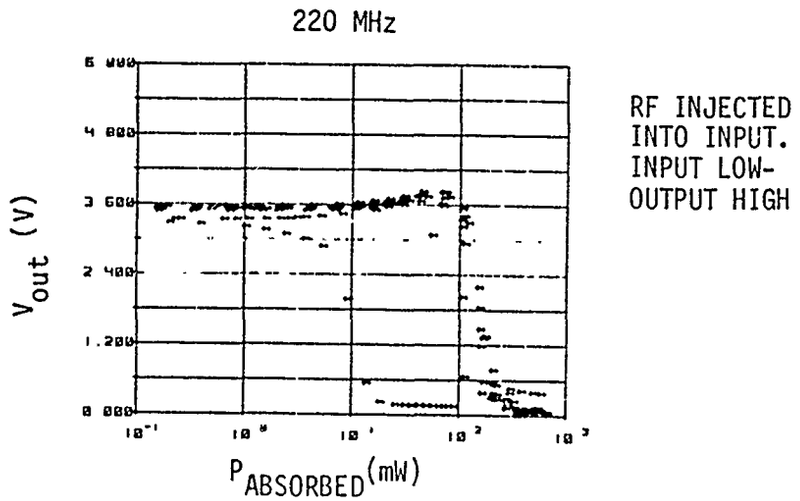


(a) Configuration #1

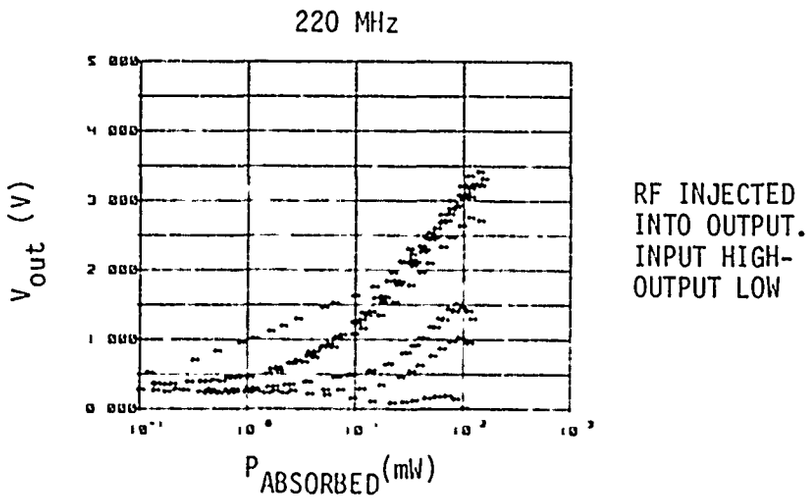


(b) Configuration #2

Figure 2 7400 Pulse Interference Test Configurations



(a) Configuration 1

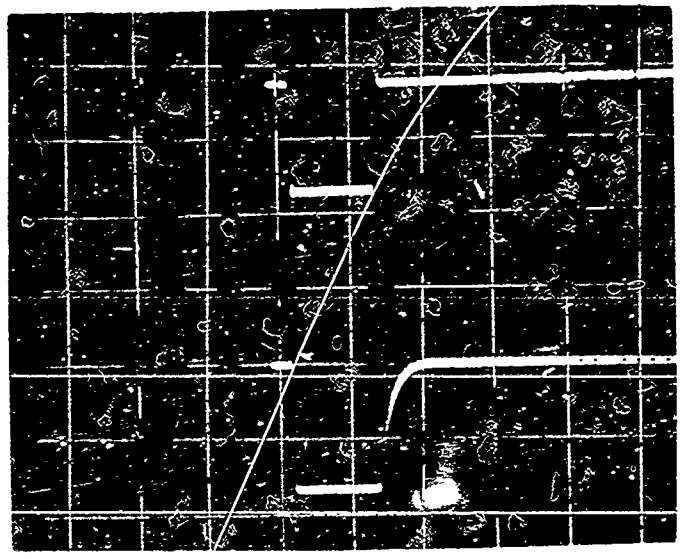


(b) Configuration 2

Figure 3 Typical CW Output Response of 7400 NAND Gate for the Two Configurations Used in Pulse Studies.

RF Into Input Port, Output High

.91 GHz



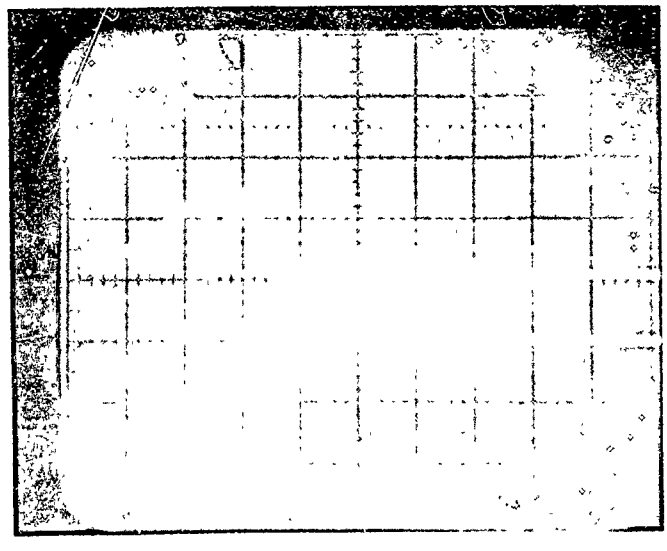
V_{out} $(\frac{2V}{DIV})$

RF
PULSE
ENVELOPE

10 μsec/DIV.

RF Into Output, Output Low

.22 GHz



$V_{out}(\frac{2V}{DIV})$

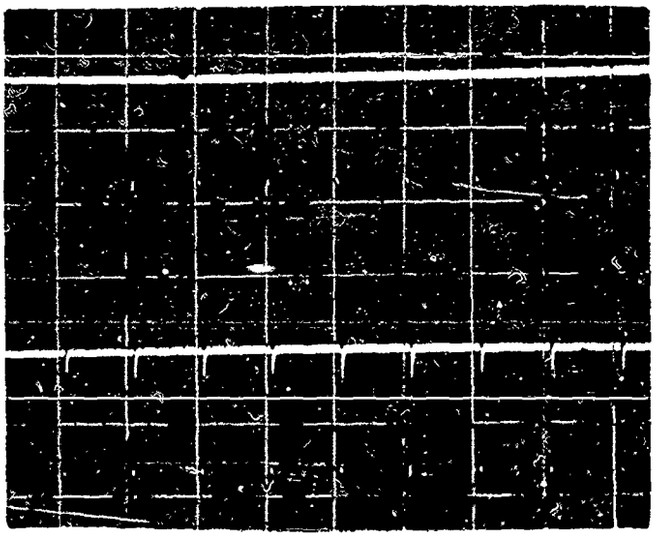
RF
PULSE
ENVELOPE

200 nsec/DIV

Figure 4 Typical Pulse Interference Effects on 7400 NAND Gate

RF Into Input Port, Output High

.91 GHz



$V_{out}(\frac{2V}{DIV})$

RF
PULSE
ENVELOPE

100 μsec/DIV.

Figure 5 Typical Pulse Interference Effects on 7400 NAND Gate Due To RF Pulses with 1 μSEC PUlse Width, 10 KHz Rep Rate

Table 1 Summary of Pulse Effects in 7400 NAND Gate

Frequency	Minimum Pulse Width	Maximum PRF	Remarks
.22 GHz	< 1μS	> 10 KHz	Peak amplitude corresponds to CW response
.91	< 1μS	> 10 KHz	
3.0	< 1μS	> 10 KHz	
5.6	< 1μS	> 10 KHz	
9.1	NOT TESTED		

2.2 741 Operational Amplifier Results - The 741 operational amplifier has previously been shown to be much more sensitive to RF interference than the 7400 [3], particularly on the two input ports (inverting and non-inverting). The 741 was operated as an inverting amplifier with gain of 10 for the CW and pulsed tests, although the pulsed testing was only carried out on the two input ports as shown in figure 6.

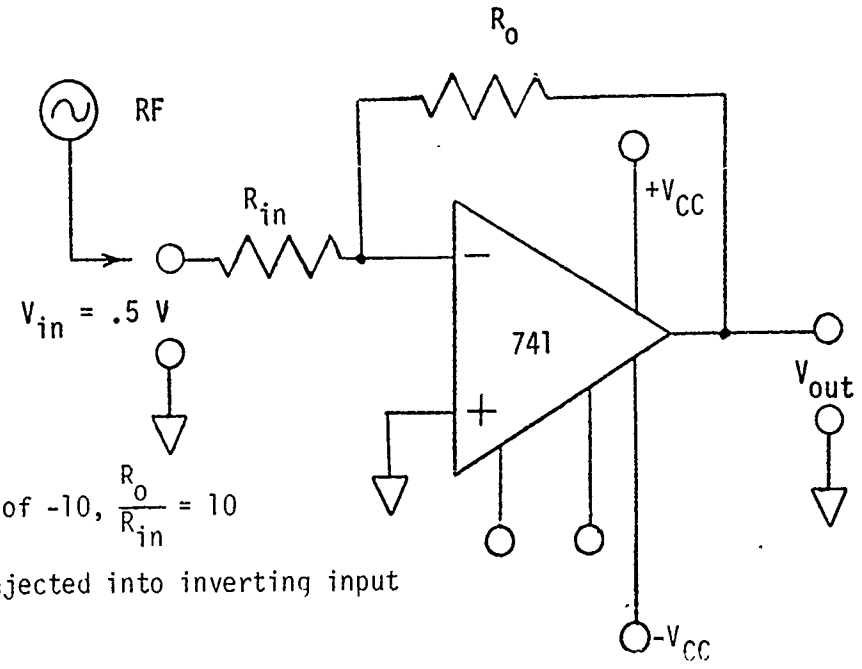
All of the interference effects observed in the 741 can be explained in terms of an offset voltage generator in the inverting input arm as depicted in figure 7 [6]. The value of the offset voltage (V_{OS}) depends upon the RF drive level as illustrated in the lower half of figure 7. For a feedback system such as we have used here, the influence of V_{OS} on the output voltage (V_{out}) can be shown to be given by

$$V_{out} = -\frac{R_o}{R_{in}} V_{in} + \frac{R_{in} + R_o}{R_{in}} V_{OS} \qquad (1)$$

Equation (1) indicates that the interference effect is a simple superposition of the interference signal and the normal device signal. Figure 8 demonstrated the excellent agreement of this model with the observed phenomena. While the value of V_{OS} at a given drive level varies with frequency and port of injection, all combinations of port and frequency (35 in all) showed this same degree of correlation with the model.

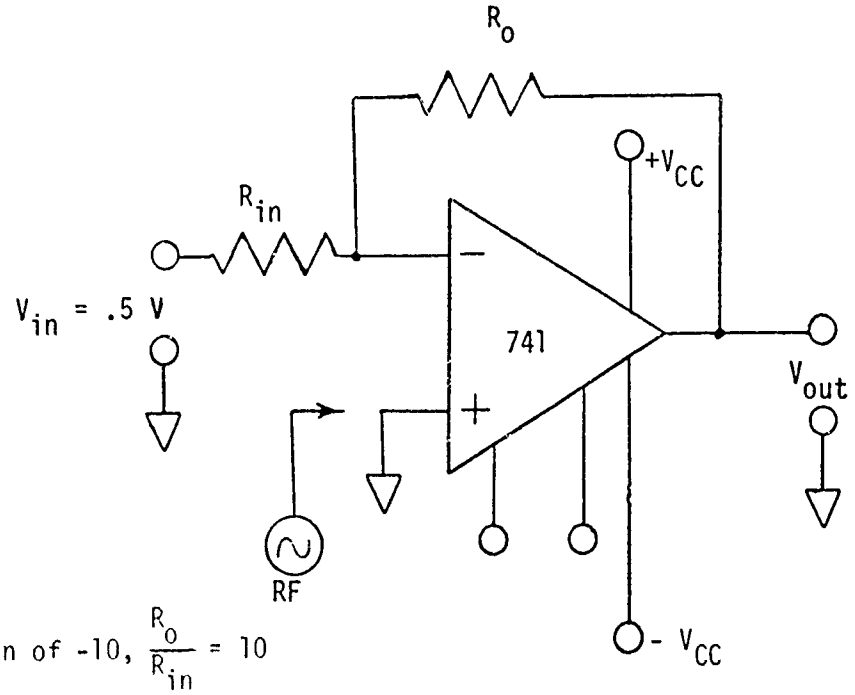
The value of V_{OS} can be positive or negative depending upon the port of injection (and sometimes the drive level). Thus, for injection into the inverting input, V_{OS} is negative; for injection into the non-inverting port, V_{OS} is positive The other ports (such as output, $+V_{CC}$, $-V_{CC}$, offset null, etc.) show a similar dichotomy and are referred to as inverting input-like and non-inverting input-like according to the sign of V_{OS}.

The output saturation limits which are determined by the positive and negative supply voltages set absolute limits beyond which the output voltage cannot



for gain of -10, $\frac{R_o}{R_{in}} = 10$

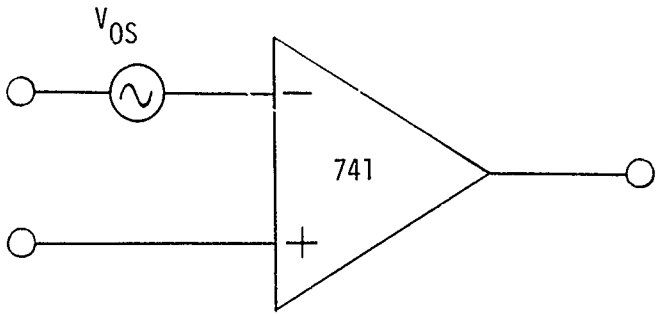
a) RF injected into inverting input



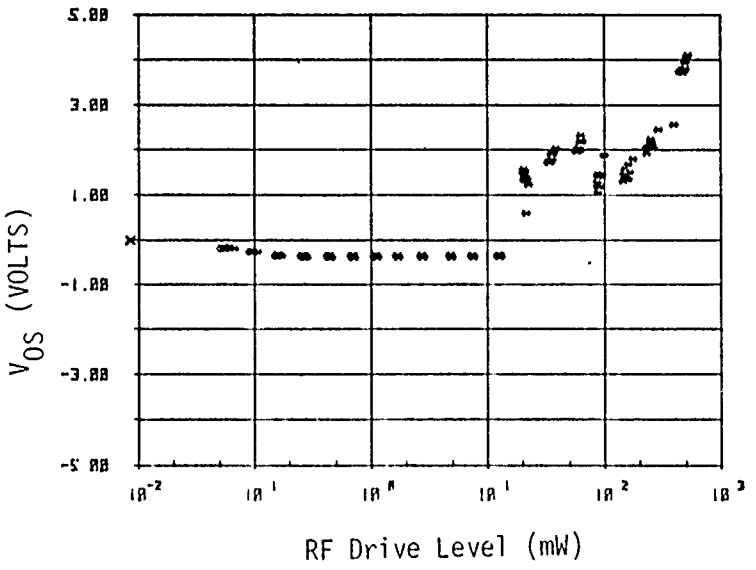
for gain of -10, $\frac{R_o}{R_{in}} = 10$

b) RF injected into non-inverting input

Figure 6 Test Configuration for 741 Pulsed Interference Tests



(a) Interference Model



(b) Functional Dependence of V_{OS} on RF Drive Level

Figure 7 Interference Model For 741 Operational Amplifier

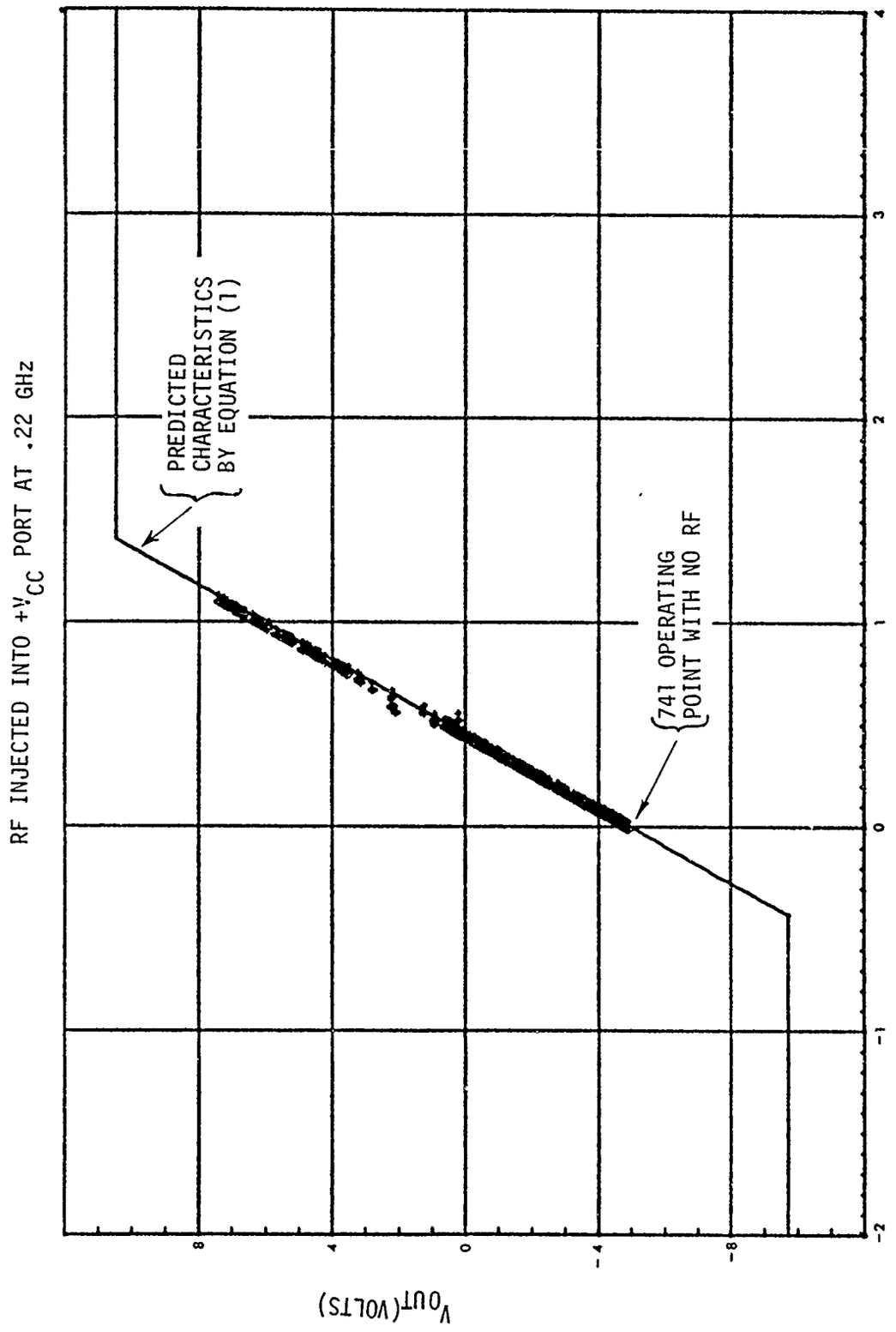


Figure 8 741 Input-Output Characteristics With RF Response Superimposed

go, either in normal operation or under RF interference conditions. This means there is a maximum RF interference effect which can be observed that depends upon the sign of V_{OS} and the value of V_{out} (under no RF). For example, if V_{out} is at $+V_{CC}$ and V_{OS} is negative (due to injection on the inverting port for instance), the maximum RF induced effect would be to drive the output all the way to $-V_{CC}$. Conversely, if V_{out} is already at $-V_{CC}$, the same interfering pulse would not even appear on the output. Figure 9 illustrates this effect by showing the manner in which an interference pulse appears superimposed on the output of the 741 under dynamic operating conditions. It is a simple matter to predict the maximum amplitude of the interference signal according to injection port and output value as shown in figure 10.

The output slew rate, which is the maximum rate the output voltage can change, sets a fundamental limit on the pulse response capability of the amplifier. For the 741 used in this study, the minimum slew rate is specified as .5 volt per microsecond. This means for interference pulses in the microsecond region, the shape of the pulse on the output will depend on both the pulse width and its amplitude. Figure 11 illustrates this effect for ideal (square) input pulses. The output pulses are either trapezoidal or triangular with rise and fall times determined by the output slew rate. Triangular pulses will not usually reach the peak value corresponding to a longer pulse width at the same power. The peak output voltage can be predicted easily by

$$V_{out}(\text{peak}) = (\text{pulse width}) \cdot (\text{slew rate}) \leq V_{out}(\text{max}) \qquad (2)$$

where: $V_{out}(\text{max})$ = value of V_{out} under long pulse or CW conditions

pulse width = duration of RF pulse

Equation (2) was verified at all test frequencies for pulse widths down to one microsecond. As with the 7400 digital device, no PRF difficulties arise up to a

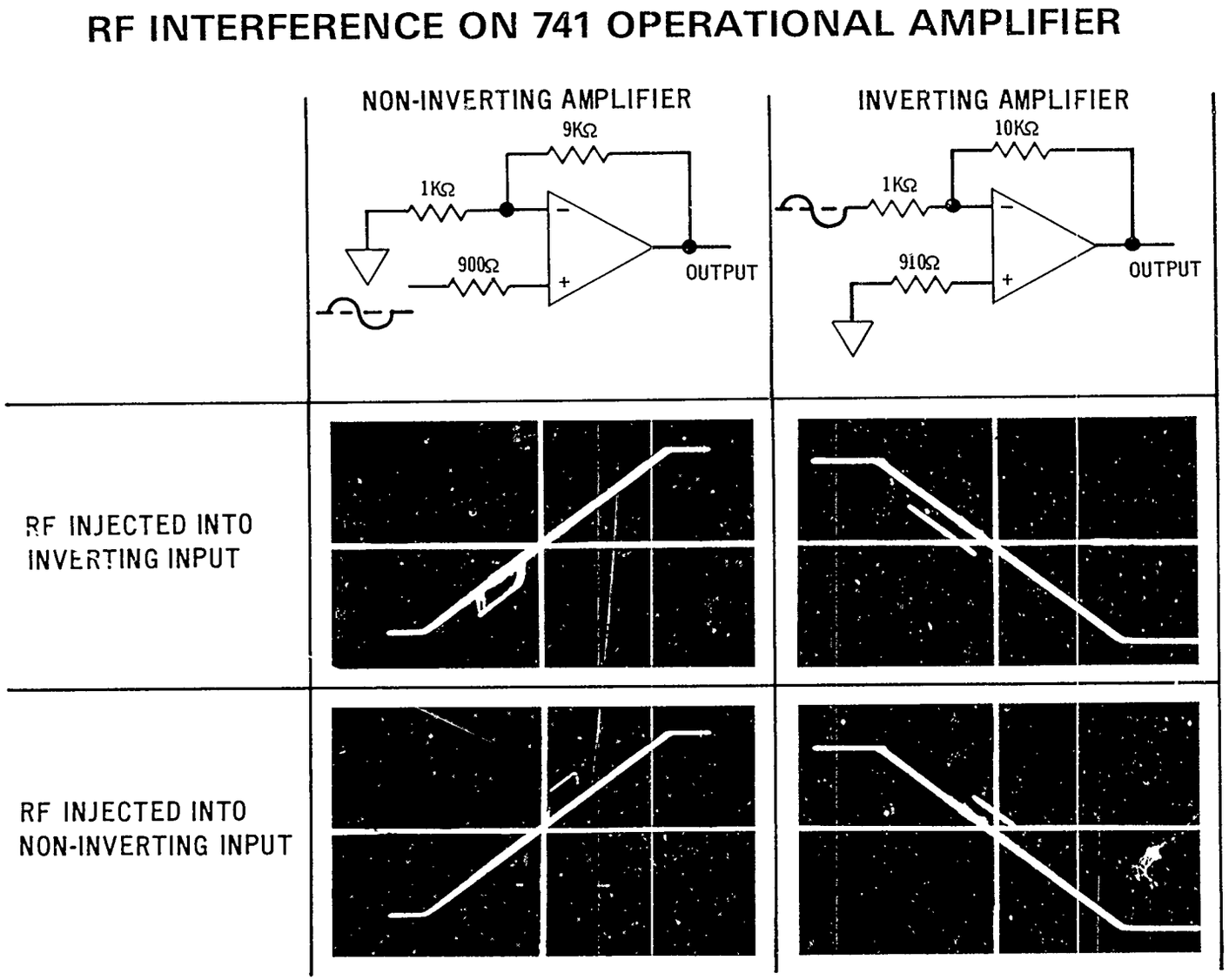


Figure 9 Typical RF Pulse Interference Effects Superimposed on Dynamic 741 Op Amp Input Output Characteristics

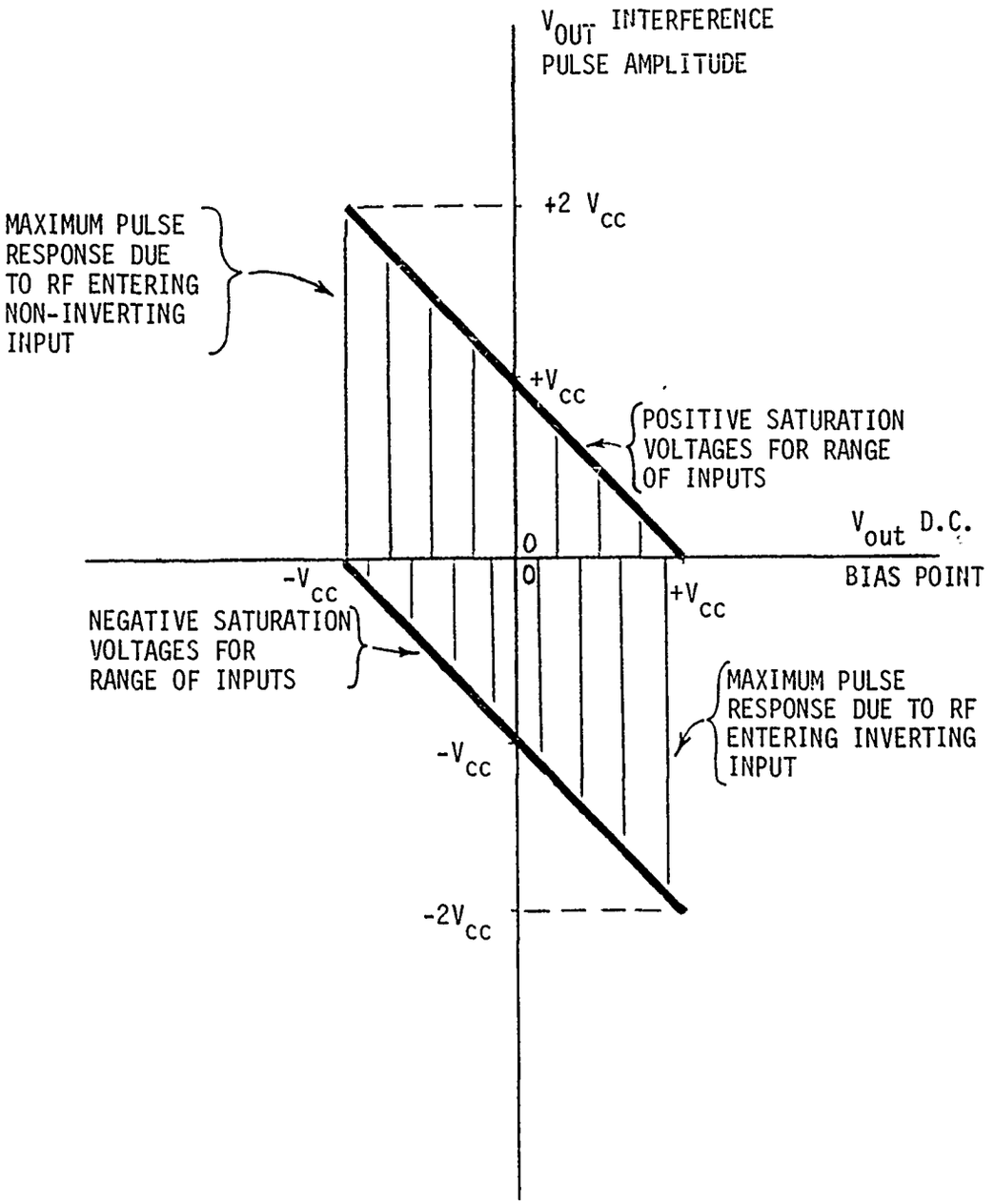
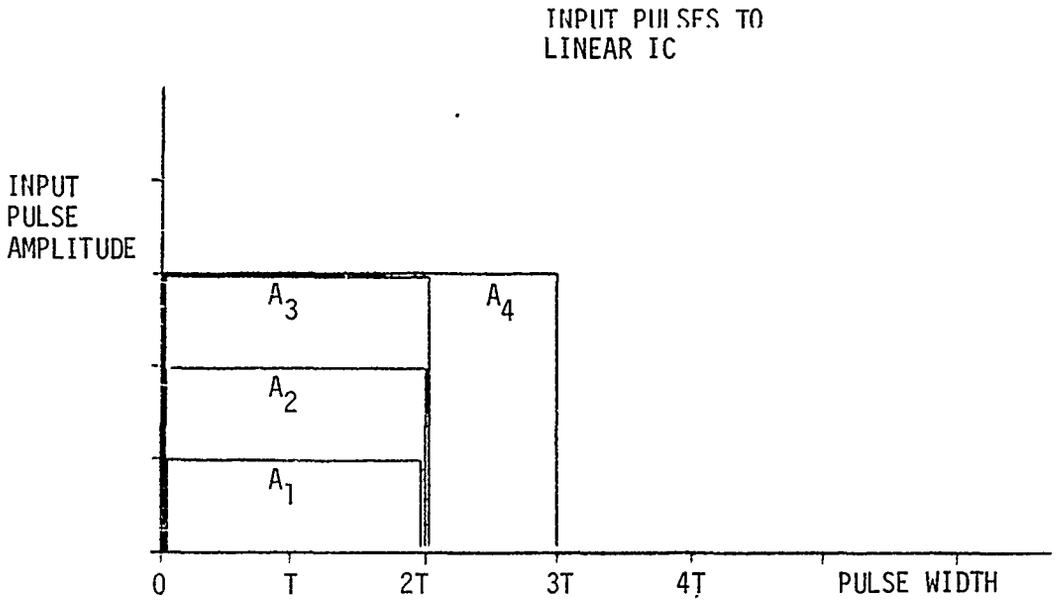


Figure 10 Pulse Interference Limits as a Function of DC Operating Point For 741 Op Amp



TYPICAL OUTPUT VOLTAGE RESPONSE OF A LINEAR IC TO ABOVE INPUT PULSES

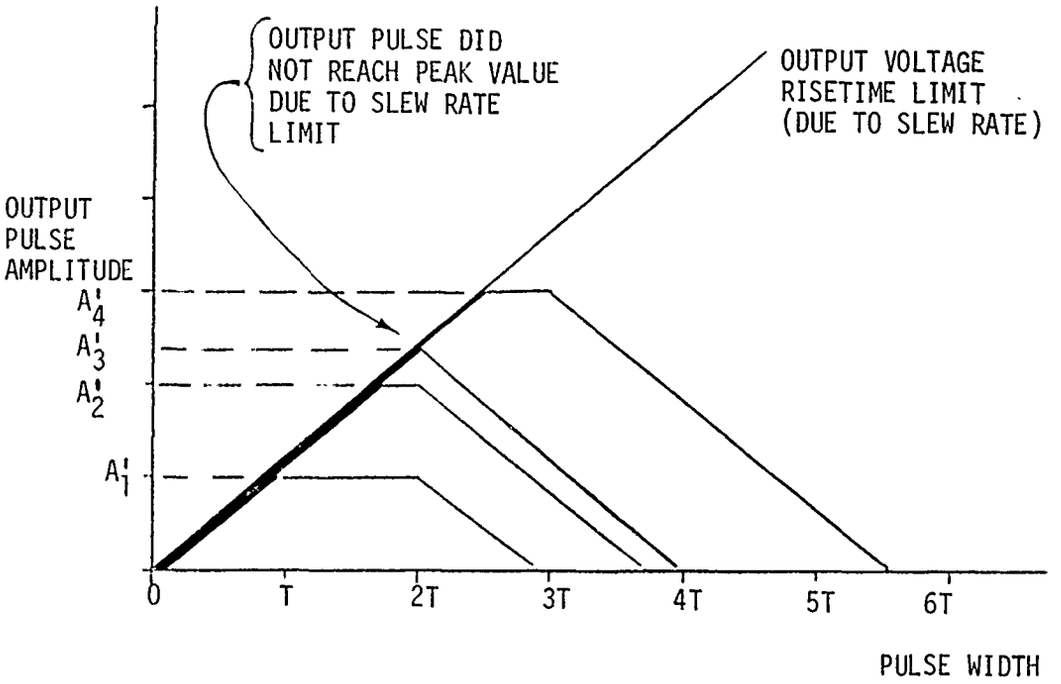


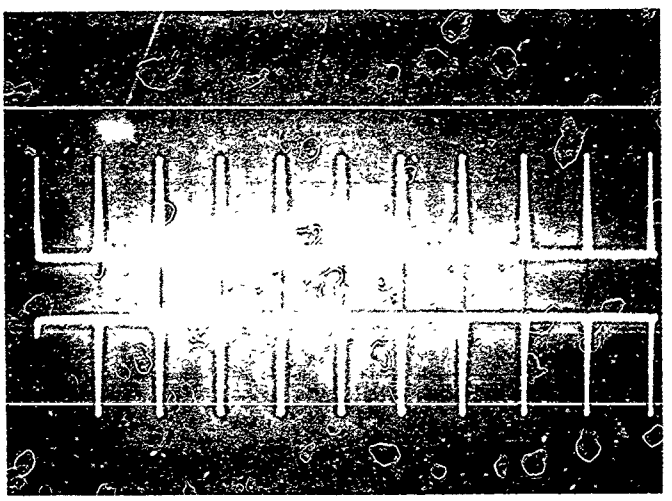
Figure 11 THEORETICAL PULSE RESPONSE OF A LINEAR I.C.

maximum rate of 10 KHz (see figure 12). Table 2 summarizes the RF induced pulse effects in the 741.

INVERTER OPERATION

RF INTO NON-INVERTING INPUT PORT

5.6 GHz



V_{OUT}

1 VOLT / DIV

RF PULSE ENVELOPE

100 μSEC/DIV

a) Pulse Interference Effects Due to RF Pulses With 1 μSEC Pulse Width, 10 KHz Rep Rate

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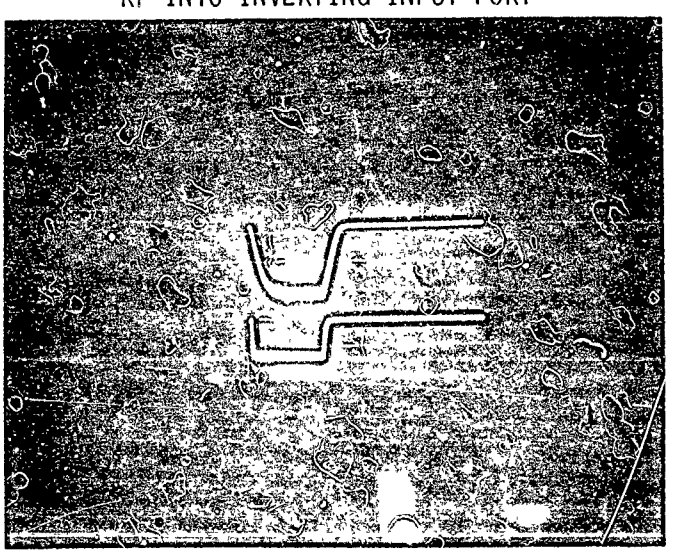
INVERTER OPERATION

RF INTO INVERTING INPUT PORT

3.0 GHz



V_{OUT}

2 VOLT / DIV

RF PULSE ENVELOPE

10 μSEC/DIV

b) Pulse Interference Effects on 741 Op Amp Due to Fast Risetime RF Pulse

Figure 12 Typical Pulse Interference Effects on 741 Op Amp

Table 2· Summary of Pulse Effects in 741 Operational Amplifiers

Frequency	Minimum Pulse Width	Maximum PRF	Remarks
.22 GHz	Depends on pulse amplitude and output slew rate. Triangular pulses can be produced to 1 microsecond.	> 10 KHz	Flat topped pulses correspond to CW value. Shorter pulses are reduced in amplitude from this value.
.91 GHz		> 10 KHz	
3.0 GHz		> 10 KHz	
5.6 GHz		> 10 KHz	

3. CIRCUIT IMPLICATIONS OF PULSED RF INTERFERENCE

Individual device response to interfering RF pulses does not provide complete information for assessment of electromagnetic susceptibility in Navy electronic systems. Rather, the chain of steps in a complete analysis leads through circuit responses, subsystem effects, and ultimately to overall system response. It is important to consider these higher effects in the components program for two reasons: the adoption of meaningful criteria for device responses depends upon their significance in the bigger picture, and communicating our results to those system designers who will eventually need them requires that we "talk their language." In this section we will discuss RF pulse response implications in the two broad categories of digital and linear devices.

3.1 Digital Circuits - Most digital circuits utilize two-state logic in which the output of devices is either "high" or "low." For whatever interpretation a designer places on these states (logical true or logical false, etc.), it is essential that he knows the results which a given set of inputs will produce at the output. There are many reasons why particular circuits may fail to produce the expected results, and these reasons range from excessive noise in the system to outright component failure. A clear cut indication of trouble is the bit error in which a "high" is interpreted as a "low" or vice versa. More subtle problems include increased probability of bit errors due to a rise in the overall noise level.

We have demonstrated that typical digital devices can be induced to change logic state under the right combination of RF power level, injection port, device bias state, etc. For a repeated interfering stimulus as would result from a pulsed radar environment, for example, the overall effect as measured by the bit error rate depends upon the information stream being processed by the circuit, the clock

rate of the information, the pulse width and pulse interval of the interfering signal, and to some extent, the relative phasing of the two pulse streams.

Figure 13 illustrates some of these concepts. A simple data stream consisting of alternating highs and lows (10101010. . .) was supplied to a 7400 NAND gate. An RF pulse injected into the input inhibits the passage of the 1's so that a bit error occurs at every other bit and the output remains low during the duration of the applied RF. Similarly, the lower half of the figure shows the case of an RF pulse injected on the output, thereby inhibiting 0's, and the output stays high for the duration of the applied RF. As before, a bit error occurs on every other bit. The maximum number of bit errors per RF pulse is given by

$$\text{Bit errors(max)} = (\text{data rate}) \times (\text{pulse width}) \qquad (3)$$

Also, the maximum bit error rate is given by

$$\text{Bit error rate(max)} = (\text{data rate}) \times (\text{pulse width}) \times (\text{PRF}) \qquad (4)$$

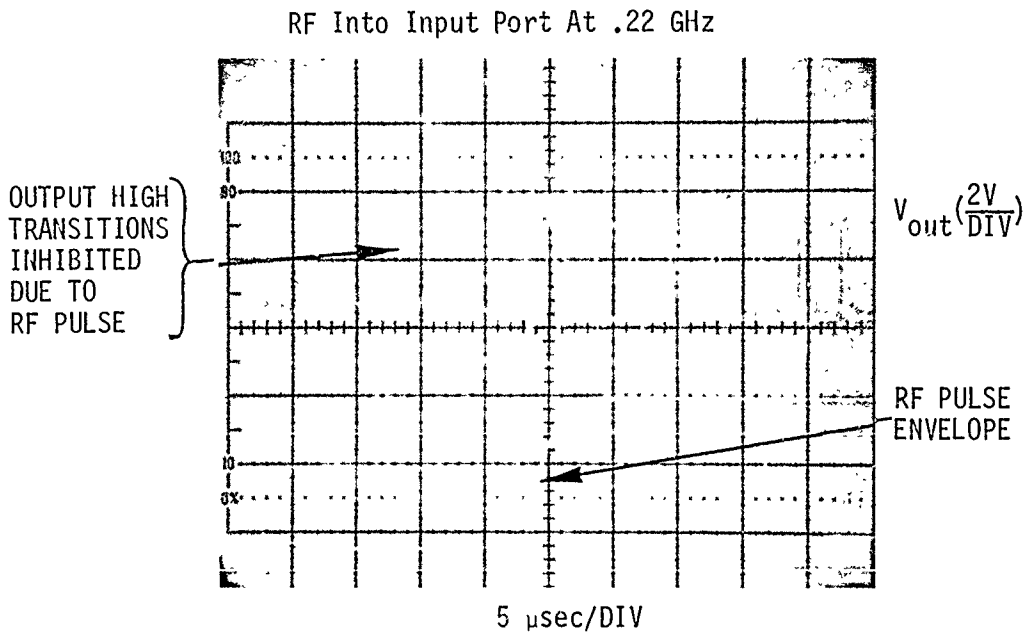
Equation (4) can be normalized by dividing both sides by the data rate term to give equation (4a).

$$\text{functional bit error rate(max)} = \text{duty cycle} \qquad (4a)$$

where: duty cycle = (pulse width) x (PRF)

The duty cycle of a radar is a commonly used figure (it gives the ratio of the average output power to peak output power) and will often fall in the region of .001. In such an environment strong enough to cause interference, a system designer could expect a bit error rate equal to .1% of his clock rate. This example is, of course, simplistic since it ignores simultaneous interference on different devices in a complex system, and also ignores the possibility of multiple emitters in the environment which would add to the bit error rate linearly.

For those cases where the RF pulse width is less than the bit pulse width, the maximum bit error per pulse is one, providing that the circuit will recognize the shorter pulses. Figures 14 and 15 show how such shorter RF pulses manifest



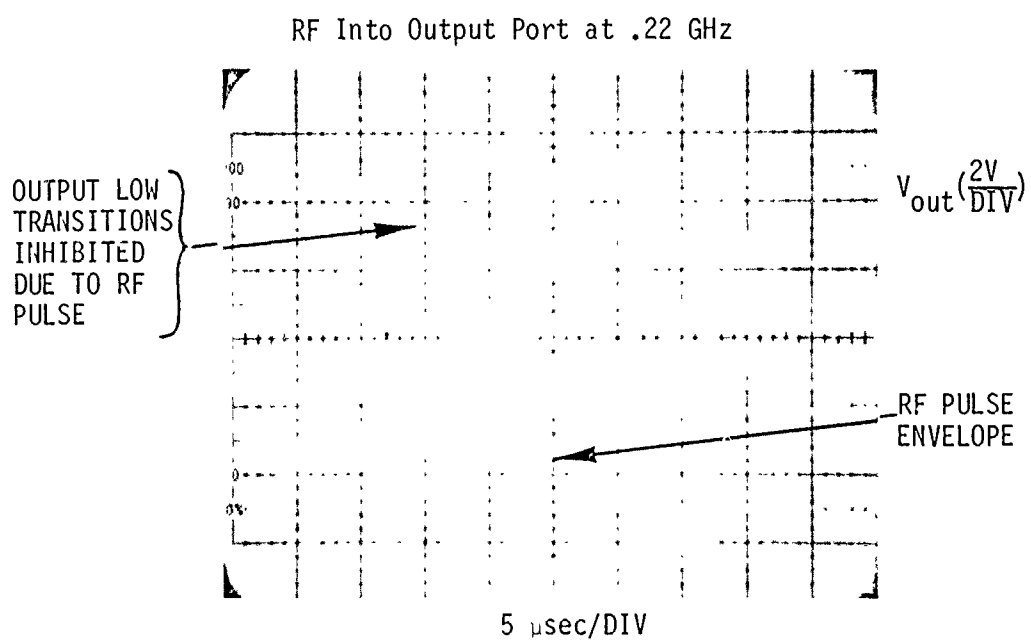


Figure 13 RF Pulse Response of 7400 Under Dynamic Conditions

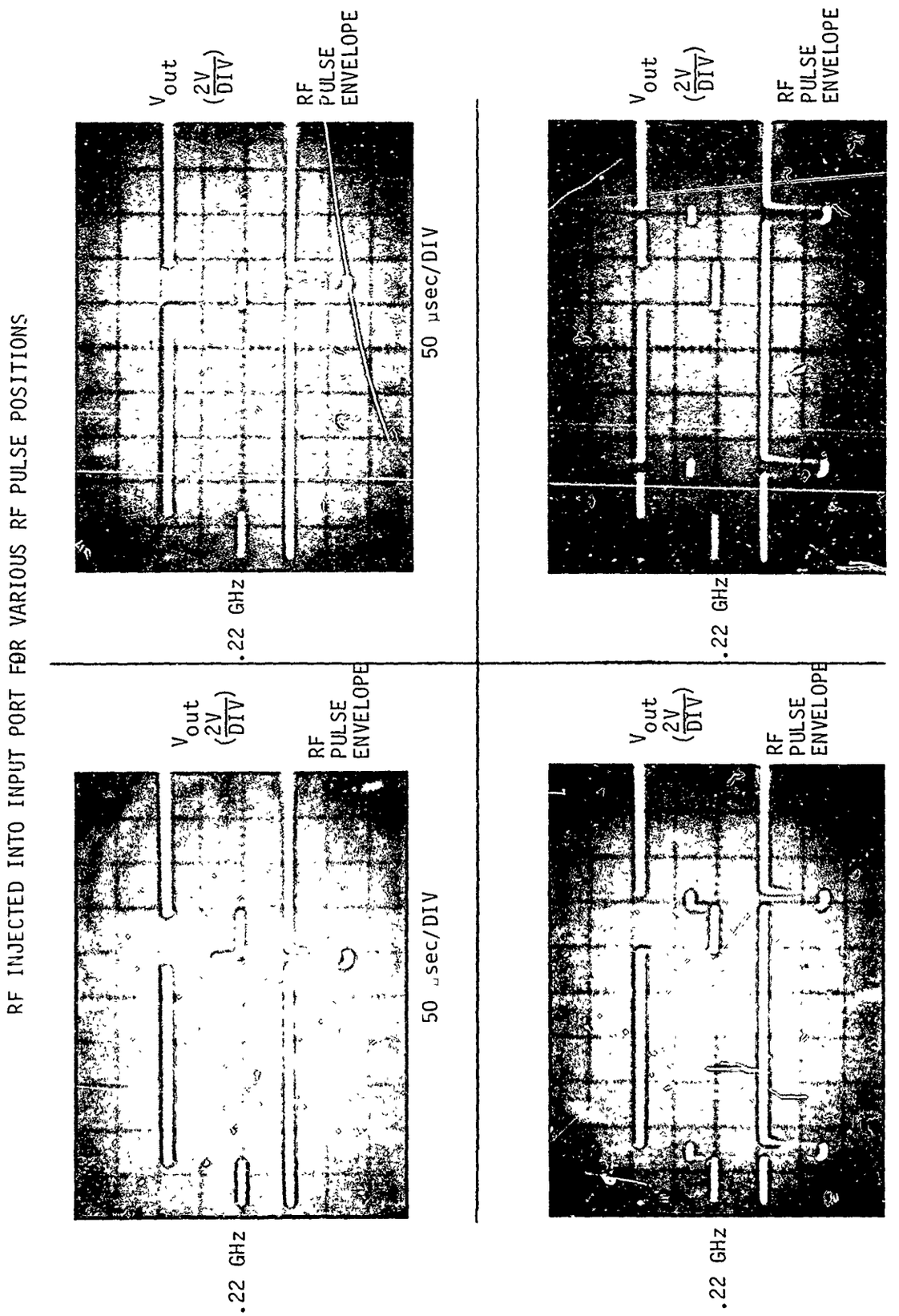
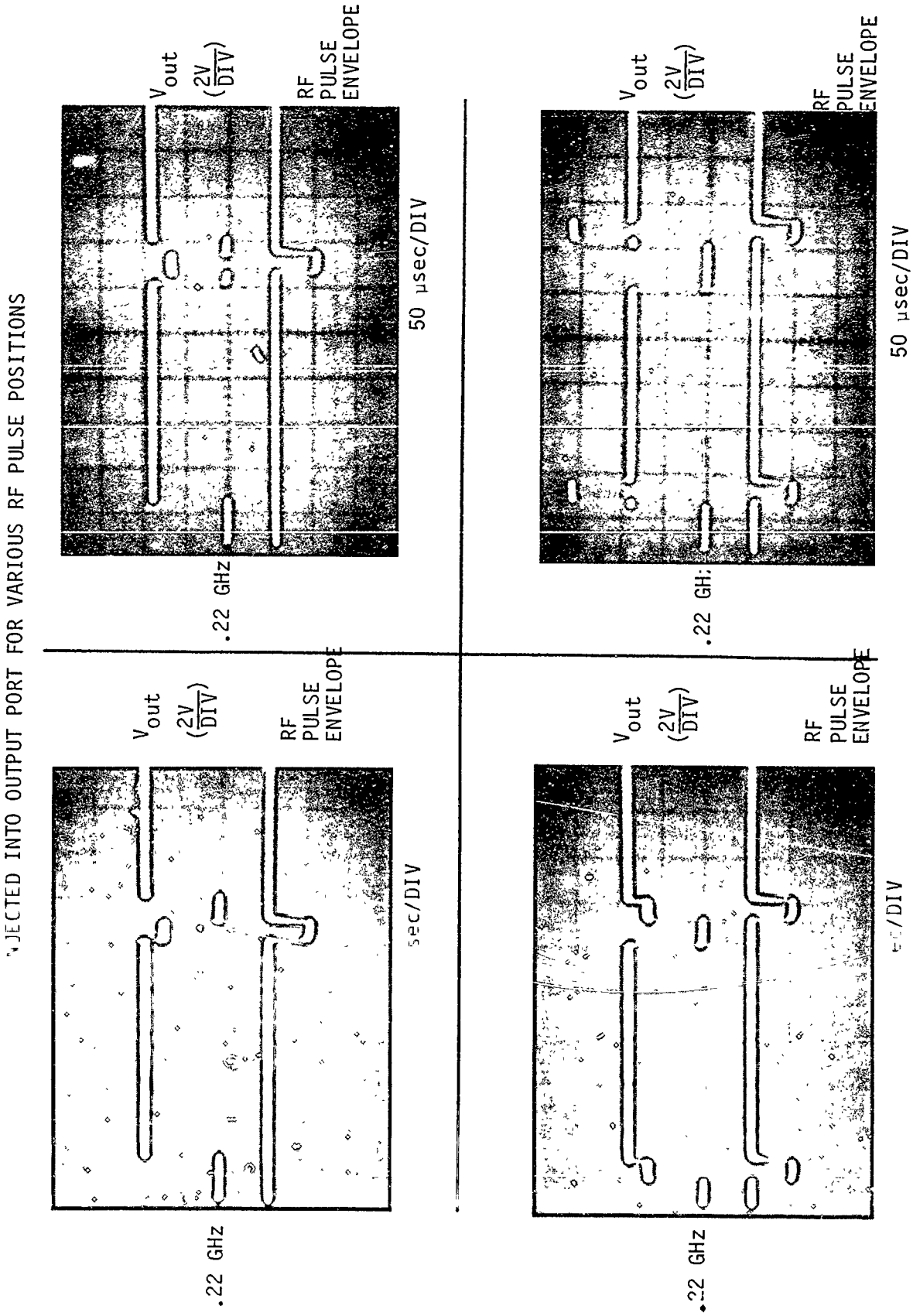


Figure 14 RF Pulse Response of the 7400 Under Dynamic Conditions



RF Pulse Response of the 7400 Under Dynamic Conditions

themselves on the data stream. It is particularly noteworthy that the effects of the interference pulse at the transition from high state to low (or vice versa) is still simply a superposition of effects (i.e., the transition point is not more or less susceptible than any other point). Such phenomena show a similarity to propagation delay problems which most system designers handle routinely.

3.2 Linear Circuits - The problem of interference pulses appearing in a linear circuit is not as clear cut as the digital case. Signal levels in linear circuits range from microvolts to tens of volts, and the effects of a given interference pulse amplitude and PRF will obviously depend upon the signal amplitude. In many circuits, especially amplifiers, the interference can be treated as noise and a degradation in the signal-to-noise (S/N) ratio can be discussed. As demonstrated in section 2.2, the interference pulse train is relatively simple and Fourier analysis will quickly identify the spectral components of the interference. The zero frequency (DC) term is easily calculated from

$$\text{Average Interference Level} = (\text{peak value}) \times (\text{duty cycle}) \qquad (5)$$

Thus, for example, an interference pulse train with peak amplitude of one volt and duty cycle of .001 will have an average interference level of one millivolt. Such an interference level would be quite serious in a low level pre-amplifier for instance, but would not even show up in a power stage. Also, many linear circuits interface with transducers, electromechanical devices, etc., which have slow response time compared to typical radar pulse widths. This class of circuits would respond to the average value only.

On the other hand, tuned circuits can be expected to "ring" when driven by short pulses, and, hence, could respond to the peak value of the interfering pulse as well as its repetition rate. Comparator circuits would also be expected to respond to the peak values of the interfering pulse (but their own inherent slew rates may limit the response as described in section 2.2).

4. CONCLUSIONS

RF interference pulses are converted to video interference pulses by a rectification process which appears to reproduce faithfully the RF pulse envelope. Subsequent effect on integrated circuits can be predicted by considering basic device limitations such as switching speed and propagation delay in digital devices and output slew rate in linear devices. Digital devices exhibit bit errors under RF stimulus which can be related to peak RF environment levels. Linear devices may respond adversely to peak environment levels depending upon the circuit, but the most common cases should respond more to the average level of the environment.

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